AiP74HC/HCT273
Octal D-type flip-flop with reset; positive edge-trigger

Product Specification

Specification Revision History：

Version	Date	Description
2012-06-A1	2012-06	New
2023-04-B1	2023-04	Update the template

Contents

1、General Description

The AiP74HC/HCT273 is an octal positive-edge triggered D-type flip-flop. The device features clock (CP) and master reset ($\overline{MR}$) inputs. The outputs Qn will assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A LOW on $\overline{MR}$ forces the outputs LOW independently of clock and data inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features:

- Input levels:
  For AiP74HC273: CMOS level
  For AiP74HCT273: TTL level
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- Specified from -40℃ to +125℃
- Packaging information: DIP20/SOP20/TSSOP20

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74HC273DA20.TB	DIP20	74HC273	18 PCS/tube	40 tube/box	720 PCS/box	Dimensions of plastic enclosure: 26.3mm×6.4mm Pin spacing: 2.54mm
AiP74HCT273DA20.TB	DIP20	74HCT273	18 PCS/tube	40 tube/box	720 PCS/box	Dimensions of plastic enclosure: 26.3mm×6.4mm Pin spacing: 2.54mm
AiP74HC273SA20.TB	SOP20	74HC273	35 PCS/tube	80 tube/box	2800 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm
AiP74HCT273SA20.TB	SOP20	74HCT273	35 PCS/tube	80 tube/box	2800 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm
AiP74HC273TA20.TB	TSSOP20	74HC273	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm
AiP74HCT273TA20.TB	TSSOP20	74HCT273	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74HC273SA20.TR	SOP20	74HC273	2000PCS/reel	2000PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing:1.27mm
AiP74HCT273SA20.TR	SOP20	74HCT273	2000PCS/reel	2000PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing:1.27mm
AiP74HC273TA20.TR	TSSOP20	74HC273	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing:0.65mm
AiP74HCT273TA20.TR	TSSOP20	74HCT273	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

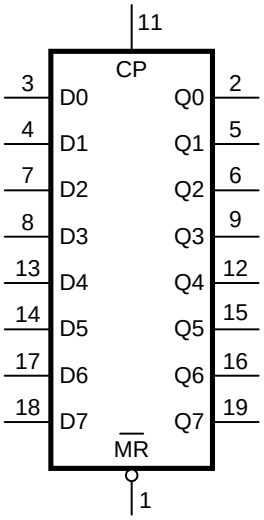


Figure 1. Logic symbol

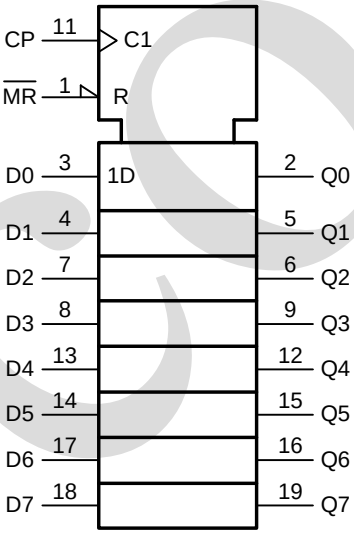


Figure 2. IEC logic symbol

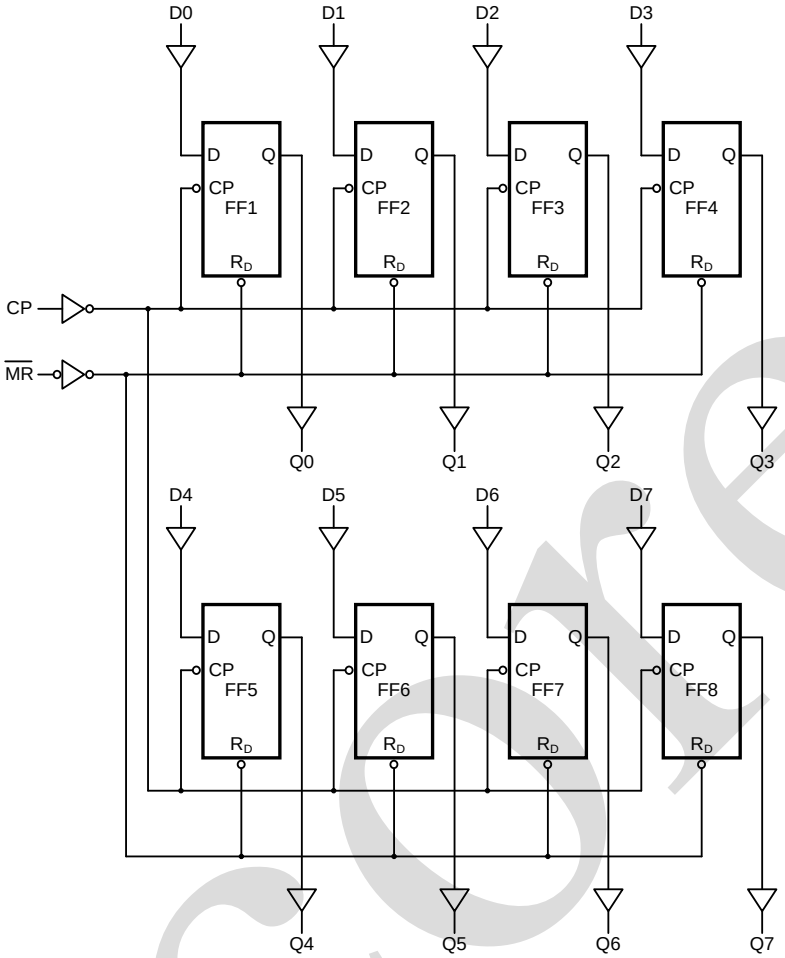


Figure 3. Logic diagram

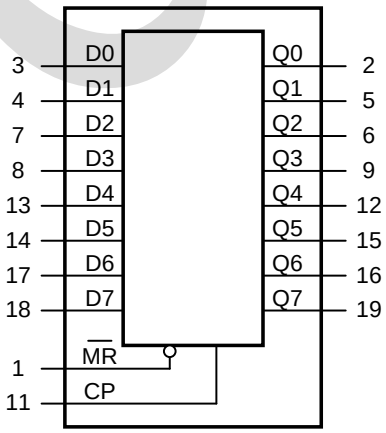
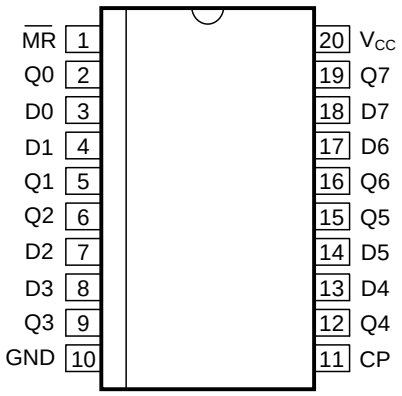


Figure 4. Functional diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	$\overline{MR}$	master reset input (active LOW)
2	Q0	flip-flop output
3	D0	data input
4	D1	data input
5	Q1	flip-flop output
6	Q2	flip-flop output
7	D2	data input
8	D3	data input
9	Q3	flip-flop output
10	GND	ground (0V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
12	Q4	flip-flop output
13	D4	data input
14	D5	data input
15	Q5	flip-flop output
16	Q6	flip-flop output
17	D6	data input
18	D7	data input
19	Q7	flip-flop output
20	V_{CC}	supply voltage

2.4、Function Table

Operating modes	Input			Output
	$\overline{MR}$	CP	Dn	Qn
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care;
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
↑=LOW-to-HIGH clock transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	-0.5V < V_O < V_{CC}+0.5V		-	±25	mA
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-50	-	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		℃

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
AiP74HC273						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+85	℃
AiP74HCT273						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	-	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	-	ns/V
ambient temperature	T_{amb}	-	-40	-	+85	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC273							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA

input capacitance	C_I	-	-	3.5	-	pF
AiP74HCT273						
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V	2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V	-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V; I_O=-20uA	4.4	4.5	-	V
		V_I = V_{IH} or V_{IL}; V_{CC}=4.5V; I_O=-4.0mA	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
		V_I = V_{IH} or V_{IL}; I_O=5.2mA; V_{CC}=5.5V	-	0.15	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V	-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V	-	-	8.0	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; $\overline{MR}$ input	-	-	360	uA
		CP input	-	-	630	uA
		Dn input	-	-	54	uA
input capacitance	C_I	-	-	3.5	-	pF

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
AiP74HC273						
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V	1.5	-	-	V
		V_{CC}=4.5V	3.15	-	-	V
		V_{CC}=6.0V	4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V	-	-	0.5	V
		V_{CC}=4.5V	-	-	1.35	V
		V_{CC}=6.0V	-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
		V_I = V_{IH} or V_{IL}; I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
		V_I = V_{IH} or V_{IL}; I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
		V_I = V_{IH} or V_{IL}; I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
		V_I = V_{IH} or V_{IL}; I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
		V_I = V_{IH} or V_{IL}; I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
		V_I = V_{IH} or V_{IL}; I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
		V_I = V_{IH} or V_{IL}; I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
		V_I = V_{IH} or V_{IL}; I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V	-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V	-	-	80	uA
AiP74HCT273						
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V	2.0	-	-	V

LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.84	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=5.2mA; V_{CC}=5.5V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V;	$\overline{MR}$ input	-	-	450	uA
			CP input	-	-	787.5	uA
			Dn input	-	-	67.5	uA

3.3.3、DC Characteristics 3

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC273							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
AiP74HCT273							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.7	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=5.2mA; V_{CC}=5.5V	-	-	0.4	V

input leakage current	I_I	$V_I=V_{CC}$ or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	$V_I=V_{CC}$ or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
additional supply current	ΔI_{CC}	per input pin; $V_I=V_{CC}$-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V;	$\overline{MR}$ input	-	-	490	uA
			CP input	-	-	857.5	uA
			Dn input	-	-	73.5	uA

3.3.4、AC Characteristics 1

(T_{amb}=25℃, GND=0V, C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC273							
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=2.0V	-	41	150	ns
			V_{CC}=4.5V	-	15	30	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	13	26	ns
$\overline{MR}$ to Qn HIGH to LOW propagation delay	t_{PHL}	see Figure 7	V_{CC}=2.0V	-	44	150	ns
			V_{CC}=4.5V	-	16	30	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	26	ns
transition time	t_t	Qn output; see Figure 6	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
pulse width	t_W	CP input HIGH or LOW; see Figure 6	V_{CC}=2.0V	80	14	-	ns
			V_{CC}=4.5V	16	5	-	ns
			V_{CC}=6.0V	14	4	-	ns
		$\overline{MR}$ input LOW; see Figure 7	V_{CC}=2.0V	60	17	-	ns
			V_{CC}=4.5V	12	6	-	ns
			V_{CC}=6.0V	10	5	-	ns
recovery time	t_{rec}	$\overline{MR}$ to CP; see Figure 7	V_{CC}=2.0V	50	-6	-	ns
			V_{CC}=4.5V	10	-2	-	ns
			V_{CC}=6.0V	9	-2	-	ns
set-up time	t_{su}	Dn to CP; see Figure 8	V_{CC}=2.0V	60	11	-	ns
			V_{CC}=4.5V	12	4	-	ns
			V_{CC}=6.0V	10	3	-	ns
hold time	t_h	Dn to CP; see Figure 8	V_{CC}=2.0V	3	-6	-	ns
			V_{CC}=4.5V	3	-2	-	ns
			V_{CC}=6.0V	3	-2	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	6	20.6	-	MHz
			V_{CC}=4.5V	30	103	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	66	-	MHz
			V_{CC}=6.0V	35	122	-	MHz
power dissipation capacitance	C_{PD}	per package; V_I=GND to V_{CC}		-	20	-	pF

AiP74HCT273							
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=4.5V	-	16	30	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
$\overline{MR}$ to Qn HIGH to LOW propagation delay	t_{PHL}	see Figure 7	V_{CC}=4.5V	-	23	34	ns
			V_{CC}=5.0V; C_L=15pF	-	20	-	ns
transition time	t_t	V_{CC}=4.5V; see Figure 6		-	7	15	ns
pulse width	t_W	V_{CC}=4.5V	CP input; see Figure 6	16	9	-	ns
			$\overline{MR}$ input LOW; see Figure 7	16	8	-	ns
recovery time	t_{rec}	$\overline{MR}$ to CP; see Figure 7; V_{CC}=4.5V		10	-2	-	ns
set-up time	t_{su}	Dn to CP; see Figure 8; V_{CC}=4.5V		12	5	-	ns
hold time	t_h	Dn to CP; see Figure 8; V_{CC}=4.5V		3	-4	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=4.5V	30	56	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	36	-	MHz
power dissipation capacitance	C_{PD}	per package; V_I=GND to V_{CC}-1.5V		-	23	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

3.3.5、AC Characteristics 2

(T_{amb}=-40℃ to +85℃, GND=0V, C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC273							
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=2.0V	-	-	185	ns
			V_{CC}=4.5V	-	-	37	ns
			V_{CC}=6.0V	-	-	31	ns
$\overline{MR}$ to Qn HIGH to LOW propagation delay	t_{PHL}	see Figure 7	V_{CC}=2.0V	-	-	185	ns
			V_{CC}=4.5V	-	-	37	ns
			V_{CC}=6.0V	-	-	31	ns
transition time	t_t	Qn output; see Figure 6	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	15	ns
pulse width	t_W	CP input HIGH or LOW; see Figure 6	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		$\overline{MR}$ input LOW; see Figure 7	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
recovery time	t_{rec}	$\overline{MR}$ to CP; see Figure 7	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
set-up time	t_{su}	Dn to CP; see Figure 8	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	73	-	-	ns
hold time	t_h	Dn to CP; see Figure 8	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	4.8	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz
AiP74HCT273							
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=4.5V	-	-	38	ns
$\overline{MR}$ to Qn HIGH to LOW propagation delay	t_{PHL}	see Figure 7	V_{CC}=4.5V	-	-	43	ns
transition time	t_t	V_{CC}=4.5V; see Figure 6		-	-	19	ns
pulse width	t_W	V_{CC}=4.5V	CP input; see Figure 6	20	-	-	ns
			$\overline{MR}$ input LOW; see Figure 7	20	-	-	ns
recovery time	t_{rec}	$\overline{MR}$ to CP; see Figure 7; V_{CC}=4.5V		13	-	-	ns
set-up time	t_{su}	Dn to CP; see Figure 8; V_{CC}=4.5V		15	-	-	ns

hold time	t_h	Dn to CP; see Figure 8; V_{CC}=4.5V		3	-	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=4.5V	24	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

3.3.6、AC Characteristics 3

(T_{amb}=-40℃ to +125℃, GND=0V, C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC273							
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
$\overline{MR}$ to Qn HIGH to LOW propagation delay	t_{PHL}	see Figure 7	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
transition time	t_t	Qn output; see Figure 6	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
pulse width	t_W	CP input HIGH or LOW; see Figure 6	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
		$\overline{MR}$ input LOW; see Figure 7	V_{CC}=2.0V	90	-	-	ns
			V_{CC}=4.5V	18	-	-	ns
			V_{CC}=6.0V	15	-	-	ns
recovery time	t_{rec}	$\overline{MR}$ to CP; see Figure 7	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
set-up time	t_{su}	Dn to CP; see Figure 8	V_{CC}=2.0V	90	-	-	ns
			V_{CC}=4.5V	18	-	-	ns
			V_{CC}=6.0V	15	-	-	ns
hold time	t_h	Dn to CP; see Figure 8	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	4	-	-	MHz
			V_{CC}=4.5V	20	-	-	MHz
			V_{CC}=6.0V	24	-	-	MHz
AiP74HCT273							
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=4.5V	-	-	45	ns
$\overline{MR}$ to Qn HIGH to LOW propagation	t_{PHL}	see Figure 7	V_{CC}=4.5V	-	-	51	ns

delay							
transition time	t_t	V_{CC}=4.5V; see Figure 6		-	-	22	ns
pulse width	t_W	V_{CC}=4.5V	CP input; see Figure 6	24	-	-	ns
			$\overline{MR}$ input LOW; see Figure 7	24	-	-	ns
recovery time	t_{rec}	$\overline{MR}$ to CP; see Figure 7; V_{CC}=4.5V		15	-	-	ns
set-up time	t_{su}	Dn to CP; see Figure 8; V_{CC}=4.5V		18	-	-	ns
hold time	t_h	Dn to CP; see Figure 8; V_{CC}=4.5V		3	-	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=4.5V	20	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

4、Testing Circuit

4.1、AC Testing Circuit

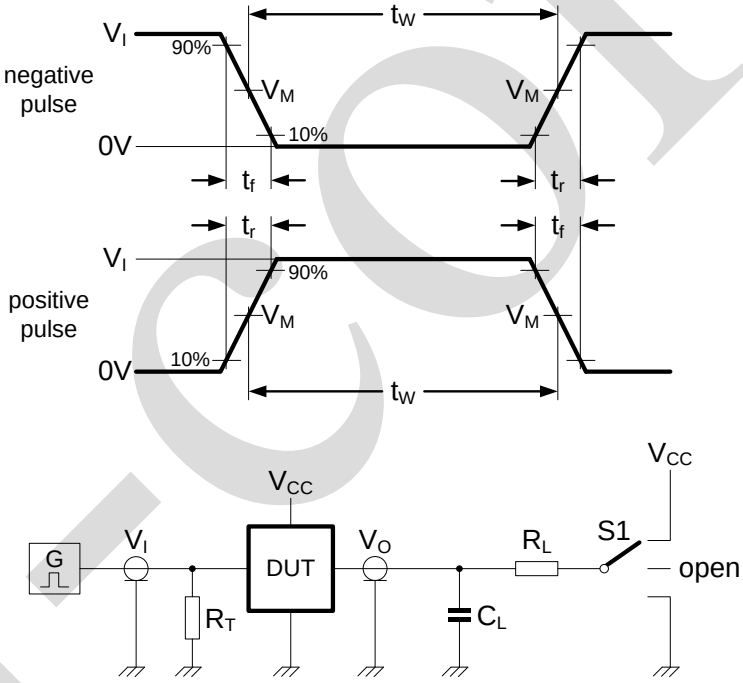


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

4.2、AC Testing Waveforms

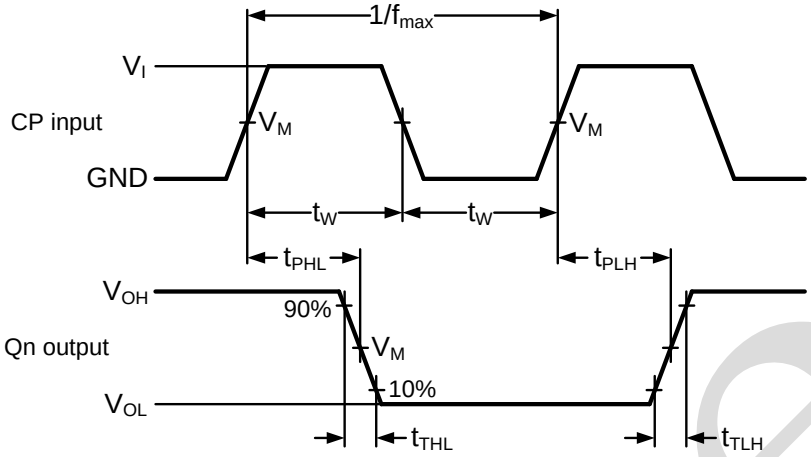


Figure 6. Propagation delay clock input (CP) to output (Qn), clock (CP) pulse width, output transition time and the maximum clock pulse frequency

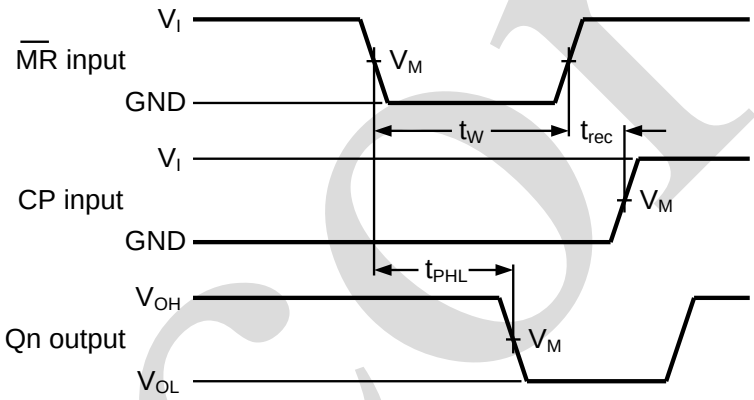


Figure 7. Propagation delay master reset ($\overline{MR}$) to output (Qn), pulse width master reset ($\overline{MR}$) and recovery time master reset ($\overline{MR}$) to clock (CP)

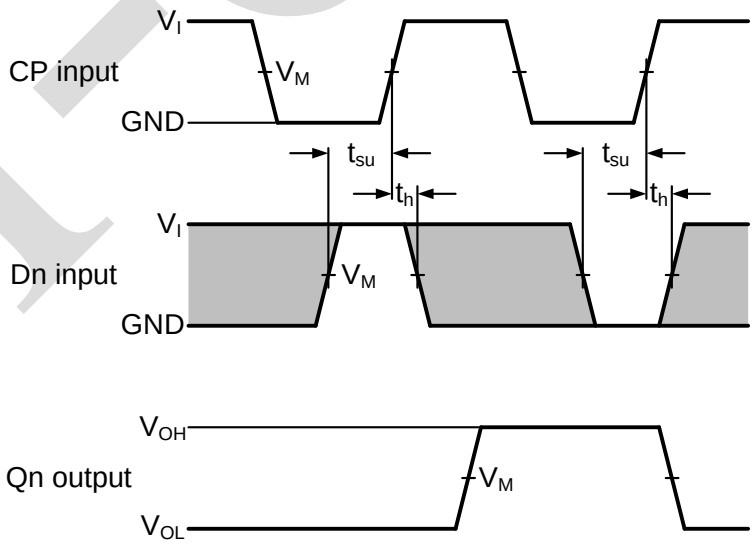


Figure 8. Data set-up and hold times data input (Dn)

4.3、Measurement Points

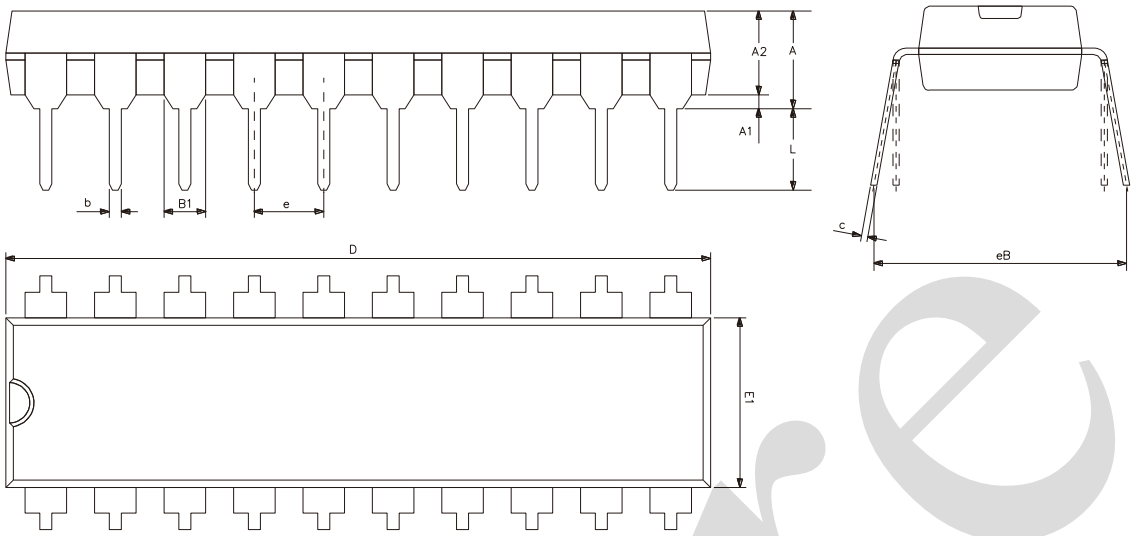
Type	Input		Output
	V_I	V_M	V_M
AiP74HC273	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
AiP74HCT273	3V	1.3V	1.3V

4.4、Test Data

Type	Input		Load		S1 position
	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}
AiP74HC273	V_{CC}	6ns	15pF, 50pF	1kΩ	open
AiP74HCT273	3V	6ns	15pF, 50pF	1kΩ	open

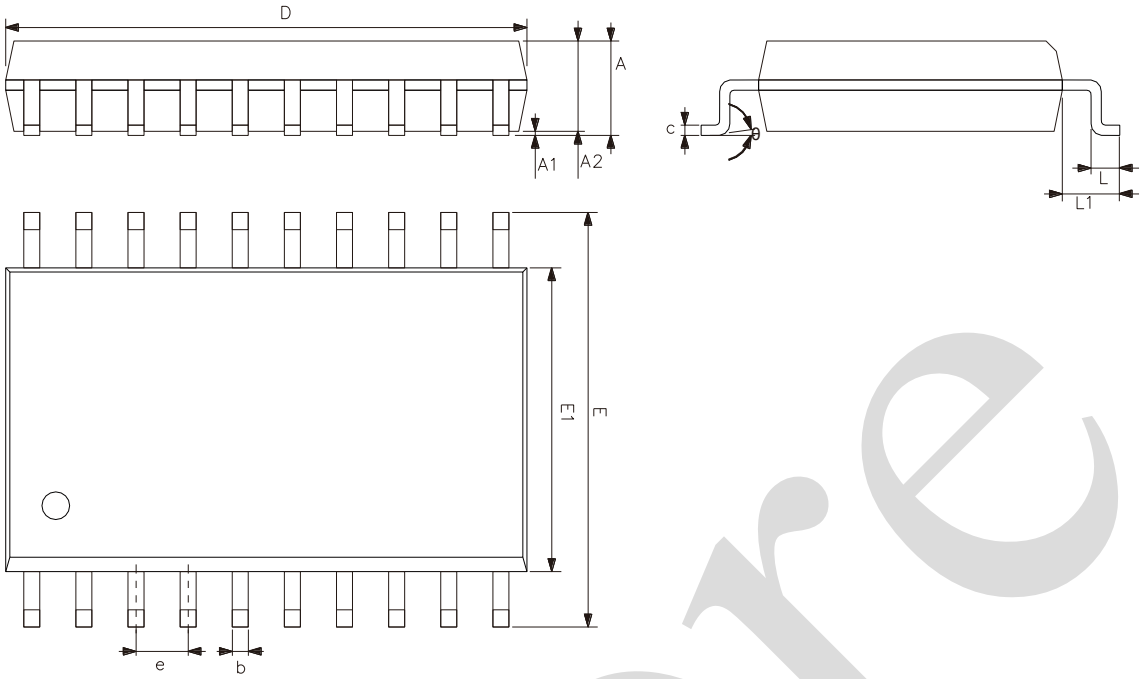
5、Package Information

5.1、DIP20



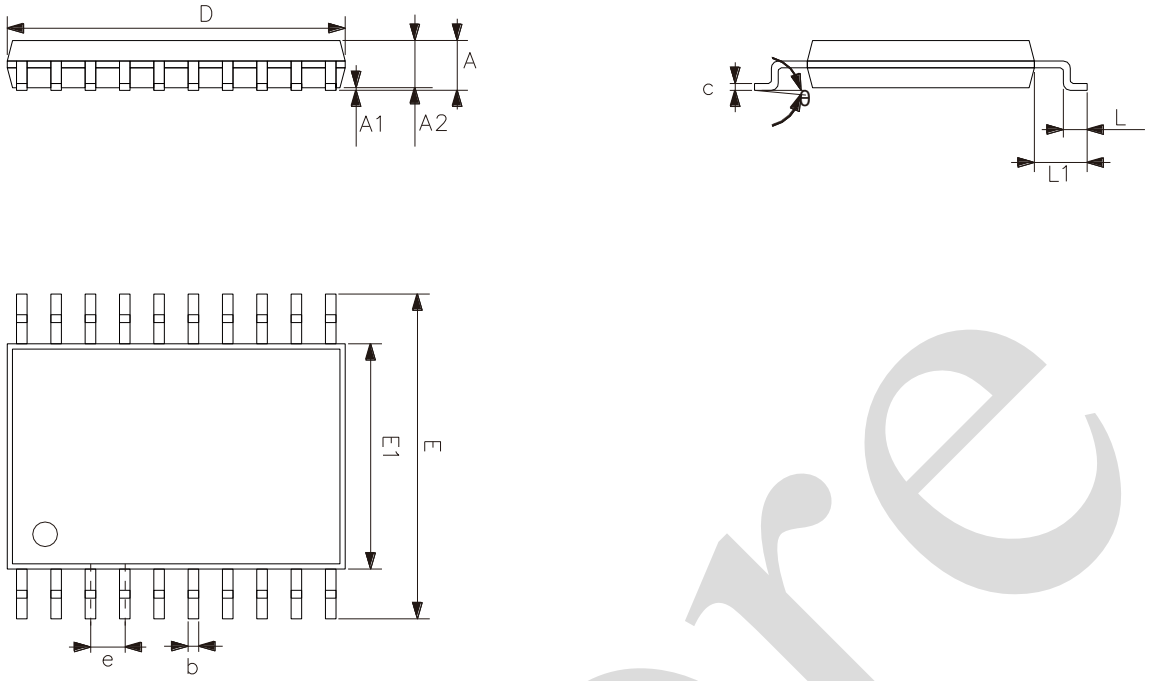
Symbol	Dimensions (mm)	
	Min.	Max.
A	3.60	5.33
A1	0.51	-
A2	3.20	3.60
b	0.36	0.53
B1	1.52	
c	0.204	0.36
D	25.70	26.54
E1	6.20	6.75
e	2.54	
eB	7.62	9.30
L	3.00	3.60

5.2、SOP20



Symbol	Dimensions (mm)	
	Min.	Max.
A	2.47	2.65
A1	0.05	0.30
A2	2.20	2.44
b	0.35	0.50
c	0.15	0.30
D	12.54	12.94
E	10.00	10.60
E1	7.30	7.70
e	1.27	
L	0.40	1.05
L1	1.30	1.50
θ	0°	8°

5.3、TSSOP20



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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